A GaAs MMIC BASED SUCCESSIVE DETECTION LOGARITHMIC AMPLIFIER

DESMOND J. NELLY and DANIEL S. PARSONS

IBM Federal Sector Division (FSD).
Owego, NY 13827-1298
USA

ABSTRACT

A six stage successive detection logarithmic amplifier (SDLA) is described in which each stage is a GaAs Monolithic Microwave Integrated Circuit (MMIC) incorporating RF amplification, detection and a novel video summation technique, using standard 0.5 micron process field effect transistors (FET) and schottky diodes. The circuit has a dynamic range of 80 dB at 3.8 GHz with linearity of ± 1 dB and power dissipation of 4.0 W.

INTRODUCTION

Logarithmic amplifiers are critical elements in EW receivers, used for encoding the amplitude of RF signals over wide input power ranges. The successive detection logarithmic amplifier offers superior performance over other logging devices in dynamic range, bandwidth and pulse response. This enhanced microwave performance is achieved by means of multiple stages of well matched devices. The GaAs MMIC process is well suited for this approach, allowing fabrication of large quantities of repeatable circuits on a single wafer.

SDLA's employing various integrated circuit technologies have been reported including Silicon [1], GaAs HBT [2], and GaAs HEMT [3]. This paper describes the development of a GaAs MMIC based SDLA using a commercially available 0.5um MESFET process. The design incorporates a novel FET distributed video summation technique which makes use of device enhancement mode characteristics.

CIRCUIT DESCRIPTION

The SDLA block diagram shown in Figure 1 differs from conventional SDLA's in video summation. Input RF power is detected by schottky diode detectors and converted to a video current via biased FETs and summed along a drain line common to all stages. This approach resembles the technique used in traditional lower frequency bipolar designs [5].

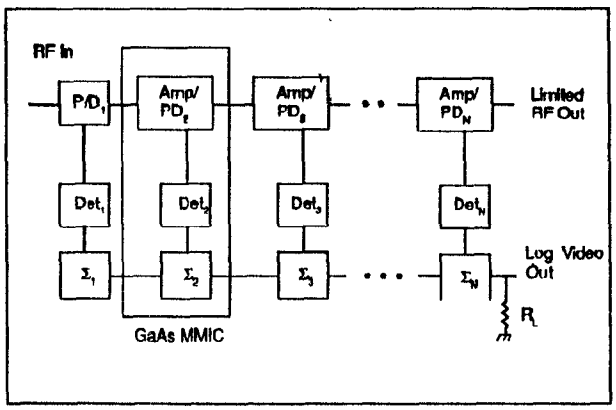

Figure 1. Successive Detection Log Amplifier Block Diagram.

The single stage MMIC schematic is shown in Figure 2. The amplifier is a two stage reactively matched design with 23 dB gain and 18 dBm limited output power at center frequency of 3.8 GHz. The amplifier output is split between a succeeding stage and the schottky diode detector circuit through a resistive power divider. Both diode D1 and summing FET Q1 are biased through off chip resistors, Rg and Rd.

92CH3162-5/92/0000-0149$01.00 © 1992 IEEE

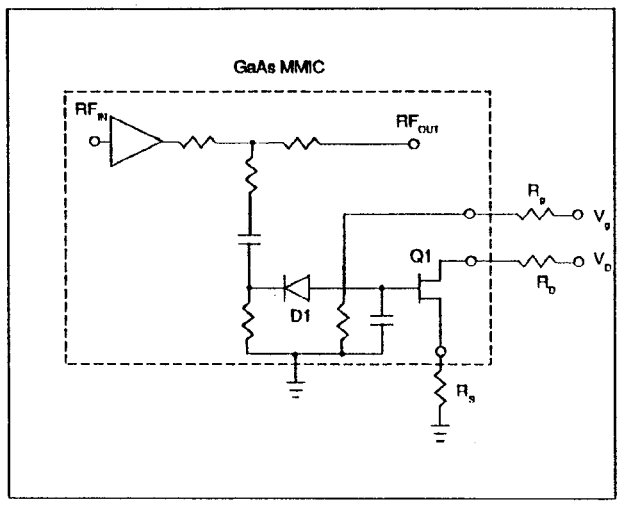

Figure 2. Amplifier / Detector Schematic.

Vg serves to forward bias D1 and place Q1 in the enhancement mode where the FET transconductance is greatest and approaches a constant value for small changes in gate-source voltage, Vgs. This configuration allows detected voltage to be converted to current by the relationship:

$\Delta Iv = Gm * \Delta Vg$, where

ΔVg = change in detector voltage over amplifier dynamic range,

ΔIv = corresponding change in FET current,

Gm = FET dc transconductance for ΔVg.

Thus each FET stage contributes (1/n)th of the total output video current.

The single stage MMIC shown in Figure 3 measures 0.080" x 0.063 ". A six stage assembly is shown in Figure 4. Due to the high amplifier stage gain, the die were separated by 50Ω transmission lines to avoid oscillations caused by positive feedback. Video currents are summed along a printed line on ceramic substrate. This line is decoupled with a low value capacitance to avoid degrading the video bandwidth.

CIRCUIT PERFORMANCE

The transconductance vs. gate source voltage for the 100um FET summing element is shown in Figure 5. The curve shows variation of less than 1.5 mS over the detector operating range (0.5V to 0.1v). The small signal gain of each stage has a

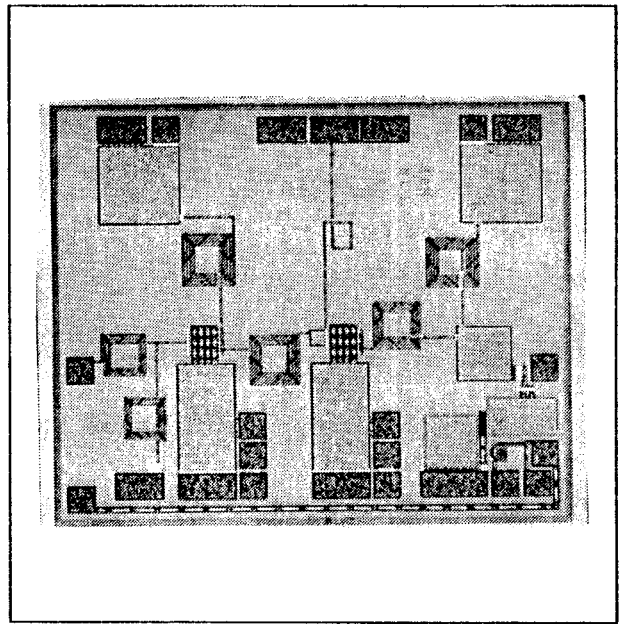
Figure 3. Single Stage MMIC Log Amp.

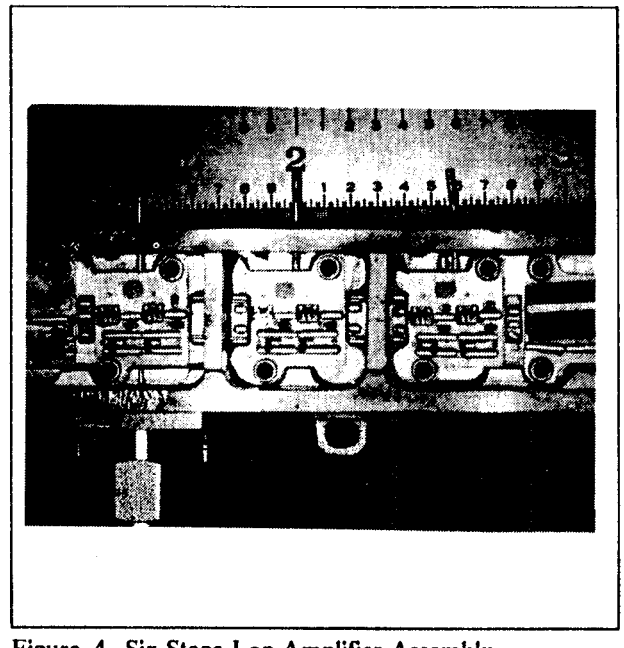
Figure 4. Six Stage Log Amplifier Assembly.

3 dB bandwidth of 1 GHz, and a useful logging bandwidth of approximately 300 MHz. The limited RF output power is 18 dBm. The output voltage and log error vs. input power for a six stage assembly is shown in Figure 6. The output voltage is referenced to a 3V drain bias on the FET summer. The measured results show a dynamic range of 80dB with ± 1 dB linearity at 3.8 GHz. The total dc power dissipation is 4 W, giving a logamp figure of merit, D = .05 W/dB.

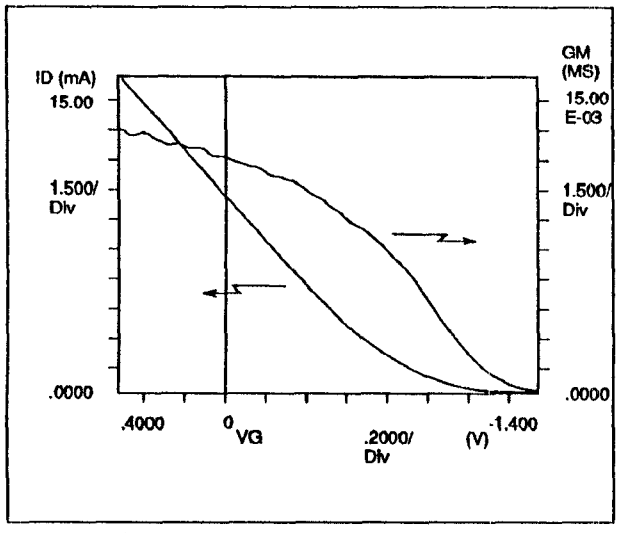

Figure 5. Video Summing FET GM vs Vg.

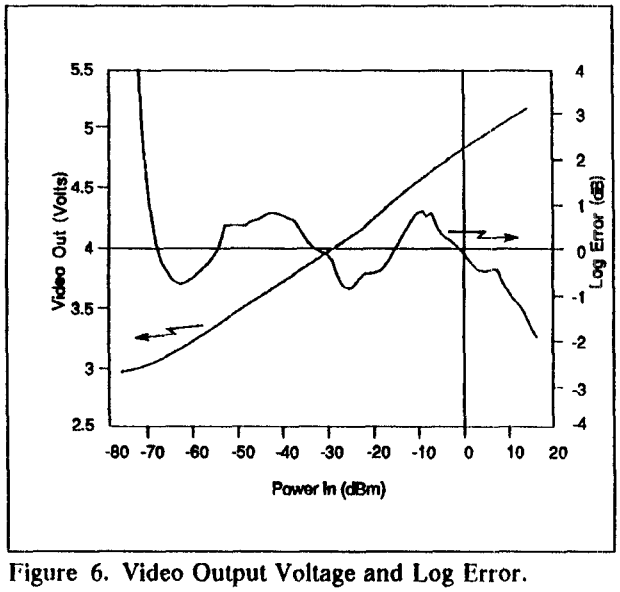

Figure 6. Video Output Voltage and Log Error.

Pulse performance and other parameters are summarized in Table 1. Receiver applications typically require further video processing for temperature compensation, offset nulling, slope adjustment and A/D conversion.

Table 1. Six Stage MMIC SDLA Performance

Parameter	Measured Value
Frequency (GHz)	3.8
Dynamic Range (dB)	80
Linearity (dB)	±1
Log Slope (mV/dB)	25
Rise Time (nS)	10
Fall Time (nS)	30
Pout (dBm)	12
Pd: (W)	4.0
D (W/dB)	0.05

SUMMARY AND CONCLUSIONS

Application of GaAs MMIC technology to successive detection logarithmic amplifiers has been achieved with excellent results. RF and video processing have been incorporated on a single die. The approach, while demonstrated for narrow bandwidth, may be applied to wider bandwidths in both RF and IF applications.

ACKNOWLEDGEMENTS

The authors would like to thank Dr. W. O. Camp and F. Owen for technical support, and L. Holmes for wafer processing and assembly.

REFERENCES

1. Tran-Nguyen, D. "An Eight Stage Log Amplifier", RF Design, November 1986, pp.84-89.
2. Gorman, G. M., et al.,"A GaAs HBT Monolithic Logarithmic IF(0.5 to 1.5 GHz) Amplifier with 60 dB Dynamic Range and 400mW power Consumption", 1989 IEEE MTT-S Digest, pp.537-40.
3. Menlo Industries, Inc., Fremont, Cal. Logamp Catalog, 1989.
4. R. S. Hughes, "Logarithmic Amplification for Passive direction Finding in the 1990's", AGARD Conference Proceedings No. 482, May 10, 1990.
5. R. S. Hughes, "Logarithmic Amplification, Dedham, Ma. : Artech House, 1986.